AMENDMENTS TO THE CLAIMS

Claims 1-18 are pending. Please amend claims 3, 5, 8, 9, 13 and 17 as set forth below. A complete listing of the current pending claims is provided below and supersedes all previous claim listing(s).

1. (Previously Presented) A circuit design simulator, comprising:

a stored electronic representation of a circuit design, said circuit design including at least one interface between a digital circuit and an analog circuit, said interface comprising a node at which said digital circuit provides an output and at which said analog circuit receives an input and provides either an output or no output, said digital circuit output taking on any one of several states including a digital high state, digital low state, or a high impedance state; and

at least one processor for simulating operation of said circuit design, said at least one processor dynamically determining whether to apply said output or said no output to said node according to said digital circuit output state.

2. (Previously Presented) The circuit design simulator of claim 1, wherein said at least one processor applies said output to said node when said digital circuit output is in said high impedance state, and applies said no output to said node when said digital circuit output is in said digital high state or said digital low state.

3. (Currently Amended) A method for simulating electronic activity at an analog/digital interface in a circuit design, said method comprising:

identifying an interface between a digital circuit and an analog circuit, said interface comprising a node at which said digital circuit provides an output and at which said analog circuit receives an input, said output taking on any one of several states including a digital high state, digital low state, or a high impedance state;

modeling said output as a digital output signal from said digital circuit to said node when said output is not in said high impedance state, and as an analog output signal from said analog circuit to said node when said output is in said high impedance state; ~~and~~

dynamically switching between said digital output signal and said analog output signal based upon whether or not said output is in said high impedance state; and

storing simulation information.

4. (Original) The method of claim 3, wherein attributes of said analog output signal are solved for while assuming that no current flows from said digital circuit to said node when said output is in said high impedance state.

5. (Currently Amended) A method for simulating electronic activity at an analog/digital interface in a circuit design, said method comprising:

identifying an interface between a plurality of digital circuits and an analog circuit, said interface comprising a node at which each of said plurality of digital circuits provides an output and at which said analog circuit receives an input, each said output taking on any one of several states including a digital high state, digital low state, or a high impedance state;

modeling at least one of said outputs as a digital output signal from the corresponding digital circuit to said node when said at least one output is not in said high impedance state, and as an

analog output signal from said analog circuit to said node when said at least one output is in said high impedance state; ~~and~~

dynamically switching between said digital output signal and said analog output signal based upon whether or not said at least one output is in said high impedance state; and

storing simulation information.

6. (Previously Presented) The method of claim 5, wherein attributes of said analog output signal are solved for while assuming that no current flows from said plurality of digital circuits to said node when said at least one output is in said high impedance state.

7. (Previously Presented) The method of claim 5, wherein each said output from said plurality of digital circuits are connected to a bus contention element, said method further comprising collectively resolving each said output from said plurality of digital circuits into a single output signal, said single output signal taking on any one of several states including said digital high state, said digital low state, or said high impedance state.

8. (Currently Amended) A method for simulating electrical operation at an analog/digital interface in a circuit design, said method comprising:

identifying an interface between a digital circuit and an analog circuit, said interface comprising a node at which said digital circuit either outputs a digital signal or else presents a high impedance output so as to be effectively isolated from said node, and at which said analog circuit receives an input signal at an input port;

adding a conditional output signal from said input port of said analog circuit to said node, wherein either an output signal or no output signal is applied from said analog circuit to said node; ~~and~~

simulating electrical operation at said interface by applying said output signal from said analog circuit to said node when said digital circuit presents a high impedance output, and applying said no output signal from said analog circuit to said node when said digital circuit presents a digital signal; and

storing simulation information.

9. (Currently Amended) A computer-readable medium on which is embodied a set of programmed instructions that cause one or more processors to perform a sequence of steps, said steps comprising:

identifying an interface between one or more digital circuits and an analog circuit, said interface comprising a node at which each of said one or more digital circuits provides an output and at which said analog circuit receives an input, each said output taking on any one of several states including a digital high state, digital low state, or a high impedance state; ~~and~~

modeling at least one of said one or more outputs as a digital output signal from the corresponding digital circuit to said node when said at least one output is not in said high impedance state, and as an analog output signal from said analog circuit to said node when said at least one output is in said high impedance state; and

storing simulation information.

10. (Previously Presented) The computer-readable medium of claim 9, wherein said programming instructions further cause said one or more processors to perform the step of dynamically switching between said digital output signal and said analog output signal based upon whether or not said at least one output is in said high impedance state.

11. (Previously Presented) The computer-readable medium of claim 10, wherein said programming instructions further cause said one or more processors to solve for attributes of said analog output signal while assuming that no current flows from said one or more digital circuits to said node when said at least one output is in said high impedance state.

12. (Previously Presented) The computer-readable medium of claim 10, wherein said at least one circuit comprises a plurality of circuits, and each said output from said plurality of circuits is connected to a bus contention element, said programming instructions causing said one or more processors to further perform the step of collectively resolving each said output into a single output signal, said single output signal taking on any one of several states including said digital high state, said digital low state, or said high impedance state.

13. (Currently Amended) A method for simulating a circuit design, comprising the steps of:

identifying an interface between a plurality of digital circuit outputs and an analog circuit input, wherein each of said plurality of digital circuit outputs can present a high impedance state;

modeling said interfaces by adding an output from an analog circuit receiving said analog circuit input to said interface; ~~and~~

simulating electrical operation at said modeled interface by resolving an electrical state of said interface using only the output from the analog circuit when all of said plurality of digital circuit outputs are in a high impedance state, and resolving the electrical state of said interface using one or more of said plurality of digital circuit outputs otherwise; and

storing simulation information.

14. (Previously Presented) A mixed analog/digital simulator comprising:

a simulation processor; and

said simulation processor including a computer-readable medium on which is embodied a set of programmed instructions that cause said simulation processor to simulate the operation of a design circuit, wherein said design circuit includes:

(1) a digital circuit having an output;

(2) a network electrically coupled to said digital circuit output, said network formed by electrically coupling an input of each of a plurality of circuit blocks at a network input node;

(3) said circuit blocks including at least one analog circuit having an analog circuit input electrically coupled to said network input node;

(4) said analog circuit having an input mode of operation for receiving an input signal at said analog circuit input and an output mode of operation for producing an output signal at said analog circuit input;

(5) said digital circuit output being applied to said network input node when said digital circuit is in a non-high-impedance state; and

(6) said output signal of said analog circuit being applied to said network input node when said digital circuit is in a high-impedance state.

15. (Previously Presented) The simulator of claim 14, wherein said output signal of said analog circuit is operably coupled to a plurality of digital circuit outputs using a bus.

16. (Previously Presented) The simulator of claim 14, wherein said input mode and output mode are selected automatically and dynamically according to a state of said digital circuit.

17. (Currently Amended) A method of simulating mixed analog/digital systems, comprising:

transforming an input of an analog circuit into an ioput, said ioput having a conditional output feeding back to a bus, said ioput being operable under a high-impedance input state, and said ioput capable of accepting a digital signal input and producing an analog signal output;

electrically coupling said ioput to a digital circuit output and to inputs of a plurality of additional circuits;

receiving said digital signal input at said ioput when said digital circuit output is in a non-high-impedance state; ~~and~~

applying said analog signal output at said ioput when said digital circuit output is in a high-impedance state; and

storing simulation information.

18. (Previously Presented) The method of claim 17, wherein said electrically coupling comprises coupling said ioput to a plurality of digital circuit outputs using a bus.